

Docket No.: 65933-044

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of

Naoteru MATSUBARA, et al.

Serial No.: 10/664,875

Filed: September 22, 2003

For: SEMICONDUCTOR DEVICE INCLUDING INTERCONNECTS FORMED BY  
DAMASCENE PROCESS AND MANUFACTURING METHOD THEREOF

: Customer Number: 20277

: Confirmation Number: 4231

: Group Art Unit: 2811

: Examiner: To be Assigned

**REQUEST FOR CORRECTED FILING RECEIPT**

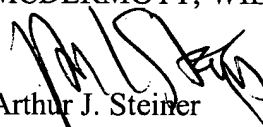
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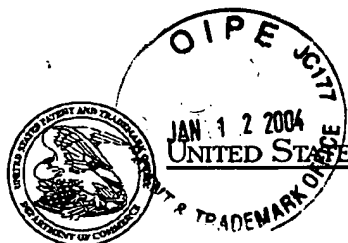
Attached is a copy of the Filing Receipt received from the U.S. Patent and Trademark Office in the above-referenced application. It is noted that the drawings information is incorrect. The drawings data should read: 5. It is requested that a corrected filing receipt be issued.

Respectfully submitted,

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/664,875	09/22/2003	2811	750	65933-044	45	17	2

CONFIRMATION NO. 4231

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FILING RECEIPT



\*OC000000011478286\*

Date Mailed: 12/12/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

**Applicant(s)**

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Kazunori Fujita, Yoro-gun, JAPAN;

**Assignment For Published Patent Application**

SANYO ELECTRIC CO., LTD.;

**Domestic Priority data as claimed by applicant**

**Foreign Applications**

JAPAN 2002-284211 09/27/2002

If Required, Foreign Filing License Granted: 12/11/2003

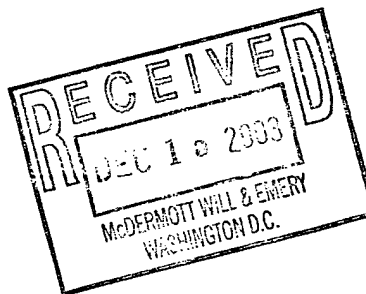
Projected Publication Date: 04/01/2004

Non-Publication Request: No

Early Publication Request: No

**Title**

Semiconductor device including interconnects formed by damascene process and manufacturing method thereof



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Title 37, Code of Federal Regulations, 5.11 & 5.15**

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